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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,305	03/25/2004	Yuichi Gomi	042262	5494

38834 7590 10/04/2007

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EXAMINER	
WANG, KENT F	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
10/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,305	GOMI, YUICHI	
	Examiner	Art Unit	
	Kent Wang	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendments, filed on 08/03/2007, have been entered and made of record. Claims 1-9 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) or rejection.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-4, 6-7, and 9 are rejected under 35 U.S.C. § 102 as being anticipated by Suzuki, US 6,975,357.

Regarding claim 1, Suzuki discloses a XY-addressing type solid-state imaging apparatus comprising:

- a plurality of pixels (pixel portion 21, Fig 1) arranged in a two-dimensional matrix (col. 3, lines 35-42); and
- a horizontal scanning circuit (horizontal scanning circuit 29, Fig 1) and a vertical scanning circuit (vertical scanning circuit 30, 31, Fig 1) for reading signals of the pixels (col. 4, lines 20-28);

- wherein vertical scanning circuit (3) concurrently selects the pixels of n rows ($\phi V1n$ and $\phi V2n+1$, Fig 11) at a first timing to concurrently effect a reset operation (through the reset transistor 16, Fig 6) of the pixels of the n rows thereof and selects at a second timing (after 1V period, Fig 11) subsequent to the first timing (at time=t1, Fig 2) the pixels of n rows of the address different from the rows selected at the first timing ($\phi V1n+2$ and $\phi V2n+3$, Fig 11) to effect a reset operation of the pixels of the n rows thereof, reset operation in this manner being repeated to effect a reset operation of all pixels (col. 6, lines 14-53).

Regarding claim 2, Suzuki discloses the pixels of the n rows concurrently selected for the reset operation to be effected are the pixels of the rows having consecutive addresses ($\phi V1n$, $\phi V1n+1$ are successively output from the first vertical scan circuit 30 and $\phi V2n$, $\phi V2n+1$ are successively output from the second vertical scan circuit 31; col. 4, lines 29-39).

Regarding claim 3, Suzuki discloses the pixels of the n rows concurrently selected for the reset operation to be effected are the pixels of the rows having discrete addresses (first vertical scan circuit 30 is put in charge of odd-number rows and the second vertical scan circuit 31 is put in charge of even number rows, Fig 11; col. 9, lines 50-67 and Fig 11).

Regarding claim 4, Suzuki discloses the vertical scanning circuit comprises:

- a row selecting section (vertical selection transistor 27*n*, Figs 1, 12; col. 4, lines 39-47)); and
- a timing pulse generating section (timing generator 32, Fig 1) to which output signals of the row selecting section ($\phi V1n$ and $\phi V1n+1$, Fig 3) and timing

signals (ϕPRD, Fig 3) are inputted to generate control signals (ϕHm, Fig 3) for effecting pixel operation (col. 4, lines 48-54 and col. 5, line 45 to col. 6, line 13).

Regarding claim 6, Suzuki discloses a row selecting section (vertical scan circuit 30, Fig 1) comprises a shift register (shift transistor, col. 4, lines 20-28).

Regarding claim 7, Suzuki discloses a timing pulse generating section (timing generator 32, Fig 1) comprises a logic circuit (AND gate 35*n*, Fig 1; col. 4, lines 48-54).

Regarding claim 9, this claim recites same limitations as claim 7. Thus it is analyzed and rejected as previously discussed with respect to claim 7 above.

Claim Rejections - 35 USC § 103

5. Claims 5 and 8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Suzuki in view of Kochi, US 2003/0112342.

Regarding claim 5, Suzuki discloses a solid-state imaging apparatus comprising a vertical scanning circuit. Suzuki does not explicitly disclose the vertical scanning circuit comprises a decoder.

Kochi discloses a vertical scanning circuit comprises a decoder circuit (col. 5, lines 49-51, Kochi). Suzuki and Kochi are analogous art because they are from the same field of endeavor of a XY-addressing type solid-state imaging sensor for an image pickup device. At the time of the invention, it would have been obvious to a person of the ordinary skill in the art to use Kochi's encoder circuit in Suzuki's solid-state imaging device. The suggestion/motivation would have been to enable the vertical scanning circuit to freely select

the pixel column selection order, thereby can realize various signal read-out orders in comparison with the shift register circuit (col. 5, lines 50-56, Kochi).

Regarding claim 8, Suzuki discloses a timing pulse generating section (timing generator 32, Fig 1) comprises a logic circuit (AND gate 35*n*, Fig 1; col. 4, lines 48-54).

Inquiries

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kent Wang whose telephone number is 571-270-1703. The examiner can normally be reached on 8:00 A.M. - 5:30 PM (every other Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc Yen Vu can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-270-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KW
28 September 2007

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER